TRIGGERERD BACK-TO-BACK DIODES FOR ESD PROTECTION INTRIPLE-WELL CMOS PROCESS

ABSTRACT

An embodiment is a Electro Static Discharge (ESD) protection device comprising: a n-doped region and a p-doped region in a p-well in a semiconductor structure. The n-doped region and the p-doped region are spaced. A n-well and a deep n-well surrounding the p-well on the sides and bottom. A first I/O pad connected to the n-doped region. A trigger circuit connected the first I/O pad and the p-doped region. A second I/O pad connected to the n-well. A parasitic bipolar transistor is comprised of the n-doped region that functions as a collector terminal, the P-well that functions as a base terminal, and the deep N-well that functions as the emitter terminal. Whereby under an ESD condition, the p-well is charged positive using the trigger circuit and the parasitic bipolar transistor can be turned on.